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The goals of this program have been taken up by major efforts at IBM Watson Research Center, Intel Portland Technology Development ,Motorola and Texas Instruments. Our program has interacted with all of these programs except for the effort at Motorola. In particular the following areas have been addressed. First, the behavior of the semiconductor-insulator interface formed between silicon and cerium oxide has been quantified. Most importantly, the trap state density, interface roughness and conduction band offset with silicon are critical parameters in determining cerium oxide's usefulness for MOS applications. Secondly, more exact knowledge of the nature of cerium oxide in thin film fonn has been ascertained in order to predict its applicability as a tunnel barrier for a silicon heterostructure.

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Final Report

# Development and Applications of Heterojunctions For Nanoelectronics for Silicon

Award Number F49620-96-0021

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# Report Summary

The development of new insulators for silicon is becoming one of major challenges facing the semiconductor industry.[1] This search is motivated by the desire to replace the venerable $SiO_2$ with an insulator that has a higher dielectric constant and the need to find insulators that might allow the fabrication of multi-layer vertical devices. This research activity has been a search for this insulator.

The goals of this program have been taken up by major efforts at IBM Watson Research Center, Intel Portland Technology Development ,Motorola and Texas Instruments. Our program has interacted with all of these programs except for the effort at Motorola.

Our efforts have surveyed a large number of possibilities. We have attempted to use $CaF_2$ but along with all of the other investigators we had little success with growing high quality silicon on the $Si/CaF_2$ structure. After a lot of efforts, we settled on the investigation of $CeO_2$ since there were indications of success in growing high quality $CeO_2$ on silicon for the high temperature superconductor efforts. The dielectric constant of $CeO_2$ is reported to be above 20.

Because of our early efforts, $CeO_2$ has become the subject of considerable attention in the field of silicon electronics because of its excellent lattice match with silicon, its insulating properties and its chemical stability. Our recent efforts have been to bring the system to the level of maturity needed for commercial devices.

In particular the following areas have been addressed. First, the behavior of the semiconductor-insulator interface formed between silicon and cerium oxide has been quantified. Most importantly, the trap state density, interface roughness and conduction band offset with silicon are critical parameters in determining cerium oxide's usefulness for MOS applications. Secondly, more exact knowledge of the nature of cerium oxide in thin film form has been ascertained in order to predict its applicability as a tunnel barrier for a silicon heterostructure.

In order to clarify the issues addressed above, a host of different types of analysis have been performed. These include but are not limited to: X-Ray Photoelectron Spectroscopy (XPS) to determine interface properties and the nature of chemical bonding in the oxide thin films, capacitance and

conductance profiling of MOS capacitor devices to examine the electrical behavior of films, various optical probing techniques to determine the optical properties of the thin films, and hybrid techniques such as photo assisted current voltage measurements to determine band gaps and band offsets of the oxide layers.

In the end, it was the aim of this project to expand the level of understanding of the silicon-cerium oxide heterojunction system to a state where it is known whether or not it has the properties necessary to be used in practical devices. Along the way it is clear that much about the nature of oxide thin films and semiconductor – insulator junctions in general has been developed

## Motivation

**Future of Silicon Electronics**

As semiconductor devices continue to scale down in size and up in speed, several fundamental physical limits begin to loom. For silicon MOS technology for instance, these limits include the minimum gate oxide thickness that can prevent gate leakage and the maximum saturation velocity of carriers in silicon that determines the operation frequency. Although alternative semiconductors provide some answers (such as III-V's for higher speed devices) for a path to circumvent these problems, there also may be some ways to extend the life of silicon itself. Below we indicate two such paths, alternative gate dielectrics and silicon-based heterostructures, both of which can be greatly facilitated by the introducion of cerium oxide materials into traditional silicon electronic device structures.

### Alternative Gate Dielectrics

Alternative gate dielectrics have been vigorously sought after as a way to avoid the gate oxide thickness problem. That is, gate insulators made out of materials with a higher dielectric constant than $SiO_2$ can be made thicker while maintaining the same device performance (same gate capacitance per unit area and same short channel behavior) in order to prevent gate leakage. In fact, Intel researchers came to the conclusion that for their purposes the most pressing physical limit standing in the way of future device scaling is the gate oxide thickness[2].

There are several candidates for possible materials to replace $SiO_2$. Buchanan[3] gives an excellent overview of the use of Silicon Oxynitrides as gate dielectrics and recently Yeo et al.[4] have succesfully made Silicon Nitride MOS devices with promising characteristics. However it is not clear how much can be gained from using nitrided oxides or pure Silicon Nitride because its band gap and band offsets with silicon are always going to be less than $SiO_2$[4] without gaining much in dielectric constant (k=7.5 for $Si_3N_4$ as compared to 3.9 for $SiO_2$). Also, while there is some knowledge about the interface state density[5] little is known about how the stoichiometry of silicon nitride and deposition conditions can affect the device.

Many other metal oxides have also been proposed. Most notable are Zirconium Oxide[6] or Yttria Stabilized Zirconium Oxide (YSZ)[7], Tantalum Oxide[8], Hafnium Oxide[9], and Titanium Oxide[10]. A comparison of the pertinent parameters for gate dielectrics of these and various other dielectrics along with those of Cerium Oxide are shown in Table I.

Table I. Comparison of the important properties of various candidates for alternative gate dielectrics.

| Material | Dielectric Const | Band Gap (eV) | CB Offset to Si (eV) | Interface Trap State Density ($cm^{-2}$ $eV^{-1}$) | Crystalline Growth | Thermodynamically Stable on Si |
|---|---|---|---|---|---|---|
| $SiO_2$ | 3.9 | 9 | 3.5 | $<1x10^{10}$ | No | - |
| YSZ | 25-29.7 [7] | ~5.8 | ~1.4 | $2x10^{11}$ [7] | Yes | Yes ? [7] |
| $ZrO_2$ | 20-25 [1] | 5.8 [1] | 1.4 (Error! Bookmark not defined.) | $3x10^{11}$ (Error! Bookmark not defined.) | No? | Yes [1] |
| $HfO_2$ | 30 [9] | 6 (Error! Bookmark not defined.) | 1.5 (Error! Bookmark not defined.) | $1x10^{11}$ [9] | No | Yes (Error! Bookmark not defined.) |
| $TiO_2$ | 40-86 [10] | 3-3.5 [10] | 1 [10] | $1x10^{11}$ [1] | No | No (Error! Bookmark not defined.) |
| $SiO_xN_y$ | 3.9-7.5 | 5.3-9 | 2.4-3.5 | ? | No | - |
| $Si_3N_4$ | 7.5 | 5.3 (Error! Bookmark not defined.) | 2.4 (Error! Bookmark not defined.) | $5x10^{11}$ [5] | No | - |
| $Ta_2O_5$ | 25 [8] | 4.4 (Error! Bookmark not defined.) | 0.3 (Error! Bookmark not defined.) (theory) 0.77 [1] (exp) | $2x10^{11}$ [1] | Yes | No (Error! Bookmark not defined.) |
| $SrTiO_3$ | 150 [10] | 3.3 (Error! Bookmark not defined.) | -0.1 (Error! Bookmark not defined.) | $6.4x10^{10}$ [1] | Yes | ? |
| $CeO_2$ | 20-26 | 5.5 [1] | 2.2 (Error! Bookmark not defined.) | $<1x10^{11}$ [1] | Yes | No (Error! Bookmark not defined.) |
| $Ce_2O_3$ | ? | 3 (Error! Bookmark not defined.) | ? | ? | Yes | Yes (Error! Bookmark not defined.) |

As one can see from the table, each dielectric has its own advantages and disadvantages. For instance, while $SrTiO_3$ has a huge dielectric constant and relatively good interface properties, it has almost no conduction band offset to Si and grows in a perovskite structure that can be very difficult to control. Or for the case of $Si_3N_4$, while it has a large (2.4 eV) band offset to silicon it has a relatively low dielectric constant and poor interface qualities. When

one looks at the cerium oxides, all of the numbers look promising except for the fact that $CeO_2$ is not thermodynamically stable on silicon at 1000 K. However it has been shown that it can be grown epitaxially on Si anyway with no amorphous $SiO_x$ layer at the interface through the use of pulsed laser deposition (PLD) at very low temperatures[11]. Also, even if the $CeO_2$ reacts with the Si, it will reduce to $Ce_2O_3$, which is thermodynamically stable on Si even at high temperatures and still acts as an insulator. In other words an ultrathin suboxide layer between the semiconductor and the $CeO_2$ will barely affect most device properties. All in all, the cerium oxides have properties that match or exceed those of all the other materials listed and yet have been studied far less than all the others in terms of its use as a gate dielectric.

## Silicon-Based Heterostructures

Different device paradigms and changes in the traditional structure of silicon devices have also been proposed as ways to further the development of silicon-based electronics. Devices that use quantum confinement have been suggested as a way to enable higher speeds and switching times. Stacking of layers of nanoelectronics has also been proposed as a way to increase device density for a given area of circuit board. To enable either of these techniques one must search for a material that can be grown as a crystal on silicon and then have single crystal silicon grown back on it. As of yet, nobody has created a true silicon heterostructure akin to those created in III-V semiconductor systems. While SiGe alloys provide somewhat of a solution, the maximum conduction band offset acheivable is very low (~0.1eV[12]) which makes using this heterojunction for quantum effects almost impossible at room temperature. An epitaxial insulator with a wide bandgap would effectively enable this technology as well as provide a true insulating substrate for growing single crystal silicon to make MOS devices (SOI). Table II is a list of some potential Si hetero-materials and their properties.

Table II: Comparison of the important properties of various candidates for silicon heterostructures.

| Material | Crystal Structure | Lattice Constant in Å (mismatch to Si) | Band Gap in eV | Conduction Band Offset (eV) |
|---|---|---|---|---|
| Si | Diamond | 5.43 (0) | 1.12 | - |
| $Si_xGe_{1-x}$ | Diamond | 5.43-5.65 (0-4%) | 0.66-1.12 | 0-0.1 |
| ZnS | Zinc Blende | 5.42 (0.2%) | 3.7 | 1.7 on (111)[1]<br>1.0 on (100)[1] |
| $BeSe_xTe_{1-x}$ | Zinc Blende | 5.63-5.15 (0-5.2%) | 2.7-4.5 | 1.3 [1] |
| $Pr_2O_3$ | Hexagonal (MnO) | | ? | |
| $CeO_2$ | Flourite | 5.41 (0.4%) | 5.5 | 2.2 |
| $Ce_2O_3$ | Hexagonal | A=3.89 (1.2% on (111) only) | 3 | ? |

Again it is clear that $CeO_2$ has properties equal or superior to those of the other materials shown above in terms of qualities for forming a silicon heterostructure. $Ce_2O_3$ is also shown to emphasize that it is not entirely non-commensurate with the Si lattice either, providing a convenient match to the hexagonal symmetry (111) face of Si. As far as experiment goes, the ZnS and $BeSe_xTe_{1-x}$ experiments carried out by Kirk et al.[13,14] have shown that fairly good epitaxial silicon can be grown on these materials. They have also shown the $BeSe_xTe_{1-x}$ system to have reasonable band offsets and electrical qualities. The example of $Pr_2O_3$ is shown above as an example of a very similar materials system in which relatively precise interfaces have been created and silicon overgrowth achieved with a good deal of initial success [15,16] but has been hardly pursued since. Very little is known about this material however and like the cerium oxides there is room for a great deal of research to determine its utility as a silicon heterojunction material.

We have already in fact shown that in some cases a high quality Si (111) epitaxially layer can be grown on an ultrathin layer of cerium oxide[17] and more recently Kim et al. [18] have succesfully regrown Si on thicker (600 Å) cerium oxide layers. In both of these cases the interface of the cerium oxide layers with the Si was not sharp; containing some $SiO_x$ and certainly some underoxidized cerium oxides. Clearly there is much room for improvement to the point where true atomically abrupt interfaces can be obtained in this system but there has been very little effort aside from some in our own group in optimizing growth conditions for this type of application.

All of these materials show incredible promise as silicon heterojunction materials and it is probably only limited time and resources that have prevented these technologies from maturing further.

**Why Cerium Oxide?**

We propose that Cerium Oxide can facilitate all of the changes in silicon based electronics suggested above.

Cerium Oxide is a wide bandgap (5.5 eV) insulator with a crystal structure that closely matches that of silicon. In its fully oxidized state ($CeO_2$) cerium oxide crystallizes in the cubic flourite configuration with a lattice constant of 5.41 Å as compared to 5.43 Å for Si. This close match enables the epitaxial growth of $CeO_2$ on Si wafers as was first demonstrated by Inoue[19]. Growth of $CeO_2$ on Si has improved in the past ten years with the advent of pulsed laser deposition which can produce highly crystalline layers at much lower temperatures than traditional MBE techniques. Studies both from the literature and our own group's research have shown that epitaxial growth can be performed at extremely low temperatures reducing the possibility of interface reactions[20] (see Fig.1). Also, $CeO_2$ melts at 2600 °C and has a Gibbs free energy of formation of -21.08 eV/molecule as compared to -17.77 eV/molecule for $SiO_2$. However as mentioned above, silicon can reduce $CeO_2$ to its suboxide $Ce_2O_3$ but no further. There is no real evidence of the formation of silicides when oxygen is present, but silicates are certainly a possiblility.

As mentioned above, an extension of traditional silicon-based electronics could be enabled with a suitable choice of alternative gate dielectric. Cerium Oxide has a dielectric constant of 26. We have measured in our lab a conduction band offset (tunnel barrier height) of approximately 2.2 eV. These two properties along with the quality of the interface discussed above make it one of the most promising alternative gate dielectrics for Si MOS.

We also suggest that Cerium Oxide could enable the paradigm shifts away from traditional device structures mentioned in the previous section. The possibility of regrowing single crystal silicon back on a $CeO_2$ layer opens up the possibility for tunneling structures such as Resonant Tunneling Diodes (RTD's), and stacked layers of silicon electronics. For these applications the issues mentioned above about the band offset and the interface quality are critical and still under study.

## History

The original motivation for growing $CeO_2$ on Si was to integrate the growth of high temperature superconducting materials with silicon. In particular, $YBa_2Cu_3O_{7-x}$ is lattice matched well to $CeO_2$. Most of the early work was focused in this direction. It was shown that high quality insulating $CeO_2$ could be grown on Si (111) wafers[19]. Since then most of the work has focused on improving the quality of this growth. Considerable strides have been made in this area including room temperature growth of $CeO_2$ on Si(111)[20] and growth on Si (100) substrates [21]. As a side note, $CeO_2$ thin films have also been successfully grown on GaAs (100)[22] and on Ge (001)[23]. However relatively little study has been devoted to the properties or feasability of realistic $CeO_2$-based devices.

## Research Under this Program

In our lab we have succeeded in growing single crystal silicon overlayers on $CeO_2$ / Si(111)[17] via e-beam MBE. Fig. 1 shows a TEM image of a section of the interface thus obtained. Although the preliminary results were quite promising they were difficult to reproduce and we could not achieve the level of sharpness at the interface as groups such as Yoshimoto et al.[11] More recently we have succeeded in fabricating stable metal / $CeO_2$ / Si capacitors that reveal an interface state density of less than $10^{11}cm^{-2}eV^{-1}$ and a DC dielectric constant of about 15 all for a nominally 500 Å $CeO_2$ film. Figure 2 is a an example of a C-V curve for such a capacitor. Further, we have been able to produce better $CeO_2$ / Si interfaces through the use of pulsed laser deposition growth at low temperatures and in low background oxygen fluxes (see Fig. 3). Finally we have succeeded in making preliminary measurements of the critical conduction band offset parameter. These measurements were made with X-Ray Photoelectron Spectroscopy and yielded a number of about 2.2 eV for $CeO_2$ on Si (111).

While we have made great strides already towards the understanding neccesary to bring cerium oxide-based device concepts to practical reality, there are still many areas where we are still limited in our comprehension of the underlying physics of this system. In general we can group these areas into two broad divisions: cerium oxide thin films and the silicon – cerium oxide interface.

**Cerium Oxide Thin Films**

In general the behavior of the cerium oxides in thin film form prior to this effort was poorly understood. We have examined how a) mode of growth and growth conditions affect the resulting stoichiometry and crystallinity of the film, b) how post-growth processing affects the films, c) what role (if any) impurities play in the oxide (for instance does silicon itself dope the oxide in such a way as to change some of its properties?), and finally d) help to address the question of how cerium's two oxidation states (III and IV) interplay including helping to reveal the nature of the empty (filled) 4f state within the bandgap of $CeO_2$ ($Ce_2O_3$). In order to accomplish these tasks we utilized all of our existing UHV growth and analysis equipment which includes: Laser, E-Beam and standard effusion cell MBE, Reflection High Energy Electron Diffraction (RHEED) and Low Energy Electron Diffraction (LEED), and XPS. A few sample XPS spectra of cerium oxides are shown in Fig. 5. Non vacuum techniques included spectroscopic ellipsometry, x-ray diffraction and atomic force microscopy. An AFM image of a cerium oxide film grown on silicon is shown in Fig. 6.

**The Cerium Oxide – Silicon Interface**

Secondly we hope to gain a better understanding of the physics and chemistry of the cerium oxide – silicon interface. This includes research on obtaining a picture of the interface at three different scales. First, the nanoscale. This includes determining what type of bonding can take place at the interface and what happens to the crystal structure of the cerium oxide grown on different silicon surfaces (different crystal directions and different pre-growth surface treatments). Second, the mesoscale, meaning what sort of materials (cerium suboxides, oxides of silicon, and silicates of cerium) can be created at the interface as function of temperature and ambient gas backgrounds. Finally, the device or macroscale. This picture should give details of the location and densities of interface trap state levels for MOS device applications. It should also give detailed information about band offsets. Essentially, all the interface information needed to understand real devices. In order to ellucidate these pictures we will again use all the UHV techniques mentioned above plus device characterization techniques such as C-V, admittance spectroscopy and photo I-V.

## Conclusion

The study of cerium oxide on silicon and devices that can be made with this heterostructure is at a critical stage. Despite some initially promising results outlined above, without more in depth analysis of the fundamental physics, this system will probably be disregarded as being too poorly understood and difficult to deal with to be of any practical use. It is the hope of this project that knowledge of this system can be advanced to the point where this is no longer true; that there is enough of a scientific knowledge base to move this materials system out of the realm of theoretical interest and technological promise into a position where the challenges become more those of the engineer than of the physicist.

**Papers Published Reporting the Principal Results of this Effort**

Jones, JT, Bridger, PM, Marsh, OJ, McGill, TC "Charge storage in CeO2/Si/CeO2/Si(111) structures by electrostatic force microscopy" J **APPLIED PHYSICS LETTERS** 75, 1326-1328 (1999).

Jones, JT, Croke, ET, Garland, CM, Marsh, OJ, McGill, TC "Epitaxial silicon grown on CeO2/Si(111) structure by molecular beam epitaxy",**JOURNAL OF VACUUM SCIENCE & TECHNOLOGY B16** 2686-2689(1998).

Preisler, E. J., Marsh, O. J., Beach, R. A., and McGill, T.C., Stability of cerium oxide on silicon studied by x-ray photoelectron spectroscopy, **JOURNAL OF VACUUM SCIENCE & TECHNOLOGY B19,** 1611—1618(2001).

Other papers are in preparation and will appear in JAP and APL.

Fig. 1,TEM of $CeO_2$ – Si interface. Taken from ref [20].

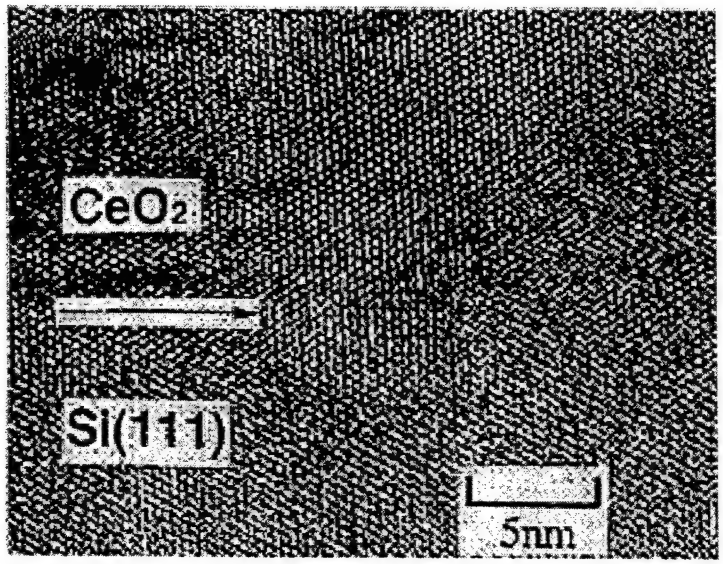



Fig.2, TEM image of Si/$CeO_2$/Si(111) heterostructure grown in our lab.

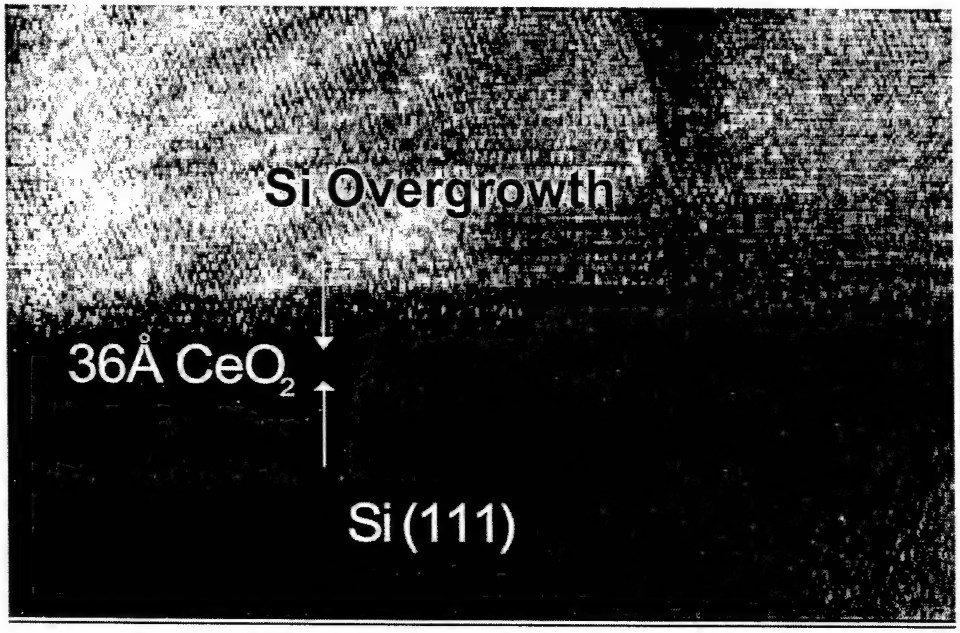


Fig. 3, C-V curve of a typical metal/$CeO_2$/Silicon MOS capacitor normalized to oxide capacitance

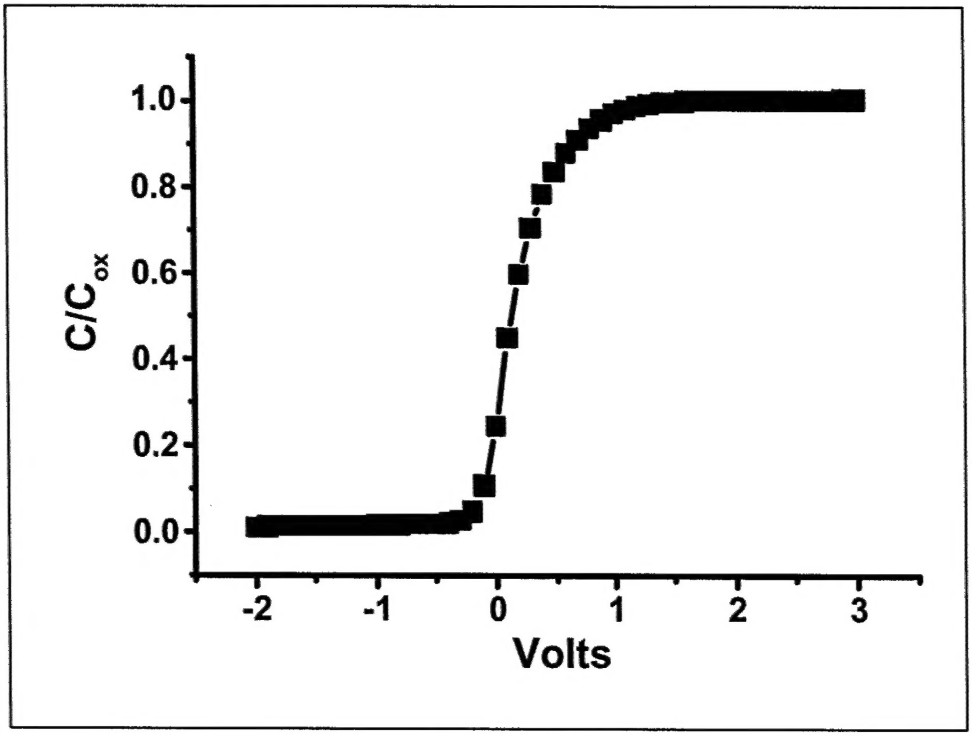



Fig.4, TEM image of a $CeO_2$ Si interface grown via PLD in our group.

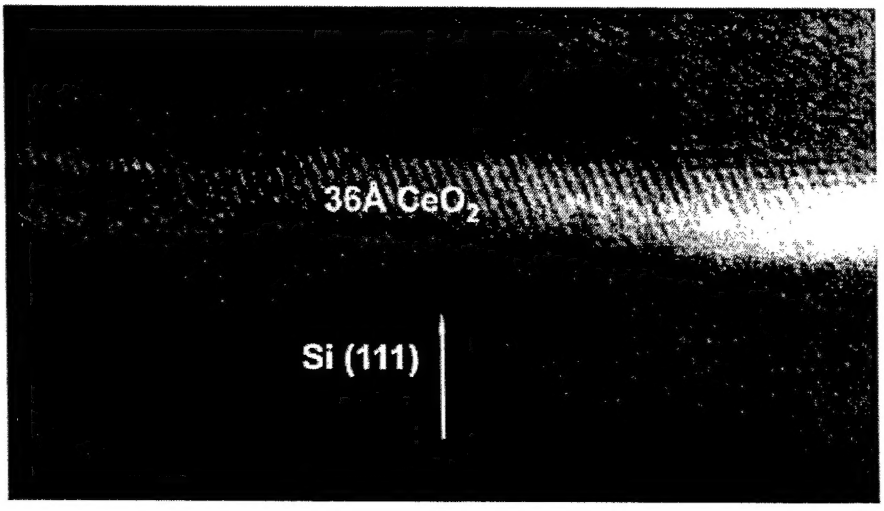


Fig. 5, Sample XPS spectra of the Ce 3d core levels in $Ce_2O_3$ (a) and $CeO_2$ (b). Also shown is the deconvolution of these spectra into their 10 peaks as discussed by Romeo et al.[24]

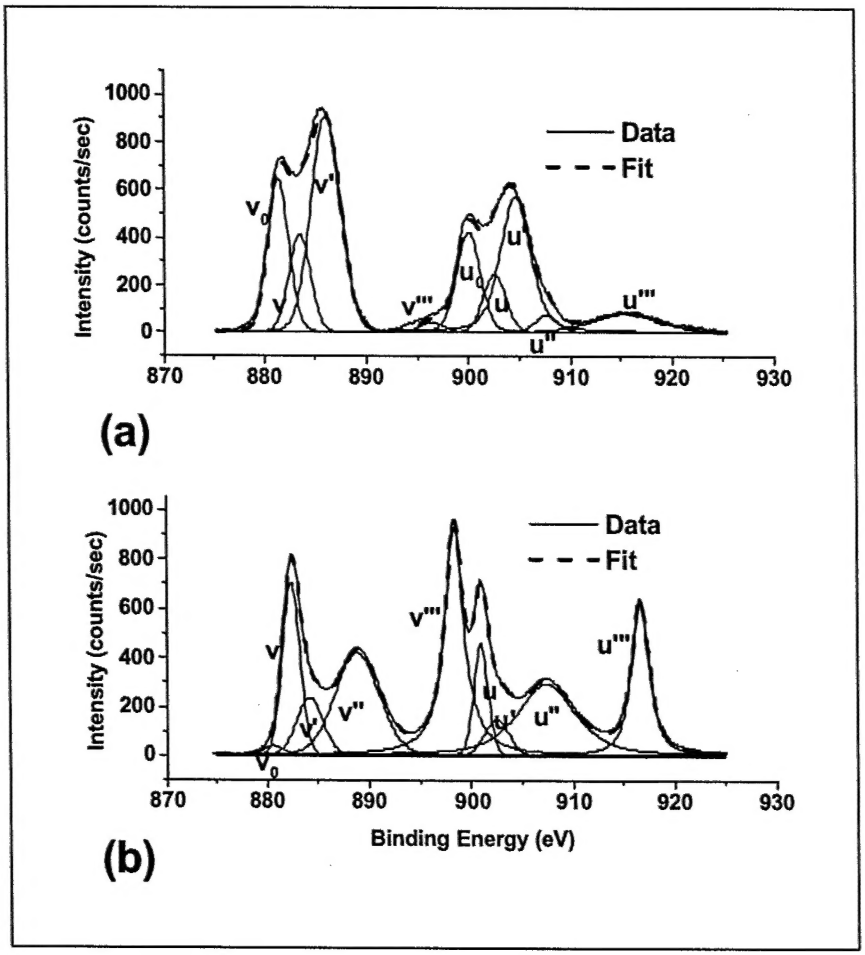
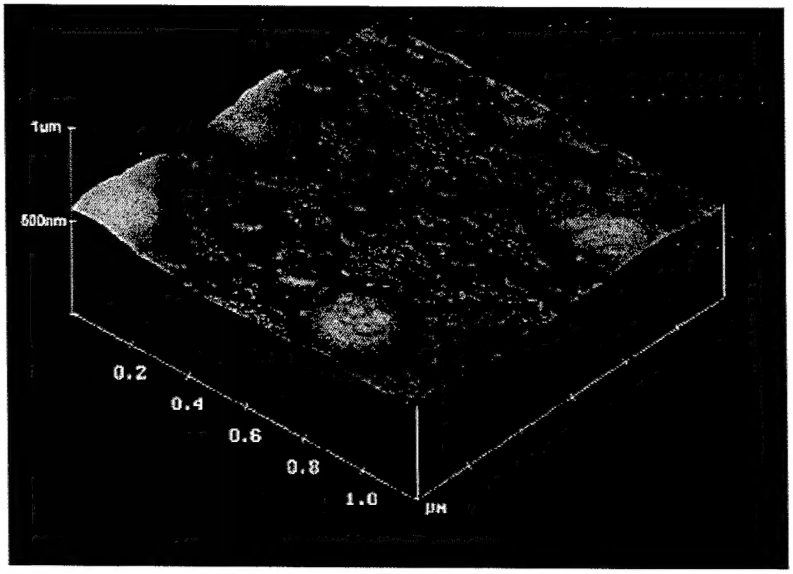



Fig. 6, AFM image of $CeO_2$ film grown on Si (111) by PLD. The features are probably all particulates created in the PLD process.



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